DERWENT-ACC-NO: 2002-308894
DERWENT-WEEK: 200235

TITLE: Wiring board for integrated circuit chip, has power supply wiring,
ground wiring and signal wiring to connect respective solder bumps to circuit
pad through respective electrode layers of capacitor

PATENT-ASSIGNEE: NGK SPARK PLUG CO LTD[NITS]

PRIORITY-DATA: 2000JP-0095178 (March 30, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2001284488 A	October 12, 2001	N/A	005	H01L 023/12

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP2001284488A	N/A	2000JP-0095178	March 30, 2000

INT-CL (IPC): H01L023/12; H05K003/46

ABSTRACTED-PUB-NO: JP2001284488A
BASIC-ABSTRACT: NOVELTY - Power supply and ground wirings (15,17) respectively
connect power supply and ground bumps (3P,3G) arranged on a wiring board (1) to
a power supply and ground pads (5P,5G) through respective power supply
electrode layers (30,32,34) and ground electrode layers (29,31,33) of a
capacitor (13), respectively. A signal bump (3S) is connected to a signal pad
(5S) by a signal wiring (19) through the capacitor.

USE - Used as motherboard for mounting integrated circuit chip.

ADVANTAGE - The cross talk noise between the signal wirings which penetrate a high dielectric layer, is reduced.

DESCRIPTION OF DRAWING(S) - The figure shows a partially enlarged sectional view of the wiring board. (Drawing includes non-English language text).

Wiring board 1

Bumps 3G,3P,3S

Pads 5G,5P,5S

Capacitor 13

Wirings 15,17,19

Ground electrode layers 29,31,33

Power supply electrode layers 30,32,34

CHOSEN-DRAWING: Dwg.2/5

TITLE-TERMS:
WIRE BOARD INTEGRATE CIRCUIT CHIP POWER SUPPLY WIRE GROUND WIRE SIGNAL WIRE
CONNECT RESPECTIVE SOLDER BUMP CIRCUIT PAD THROUGH RESPECTIVE ELECTRODE LAYER
CAPACITOR

DERWENT-CLASS: U11 U14 V04

EPI-CODES: U11-D01A; U14-H03A; V04-Q05; V04-R05A;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N2002-241787

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報**（Ａ）　(11)特許出願公開番号
特開2001－284488
（P2001－284488A）
(43)公開日　平成13年10月12日(2001.10.12)

(51)Int.Cl.⁷	識別記号	ＦＩ		テーマコード（参考）
Ｈ０１Ｌ　23/12		Ｈ０１Ｌ　23/12	３０１Ｚ	５Ｅ３４６
	３０１	Ｈ０５Ｋ　3/46	Ｑ	
Ｈ０５Ｋ　3/46			Ｎ	
		Ｈ０１Ｌ　23/12	Ｅ	
			Ｎ	

審査請求　有　請求項の数１　ＯＬ　（全５頁）

(21)出願番号　特願2000－95178(P2000－95178)

(22)出願日　平成12年３月30日(2000.3.30)

(71)出願人　000004547
日本特殊陶業株式会社
愛知県名古屋市瑞穂区高辻町14番18号

(72)発明者　徳重　和朗
愛知県名古屋市瑞穂区高辻町14番18号　日本特殊陶業株式会社内

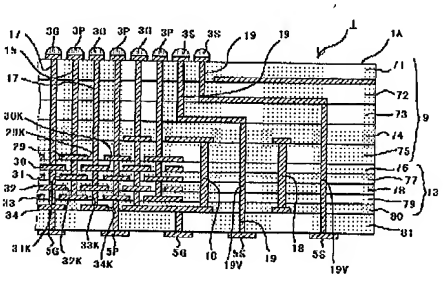
(72)発明者　木村　幸広
愛知県名古屋市瑞穂区高辻町14番18号　日本特殊陶業株式会社内

(72)発明者　黒田　正雄
愛知県名古屋市瑞穂区高辻町14番18号　日本特殊陶業株式会社内

最終頁に続く

(54)【発明の名称】　配線基板

(57)【要約】
【目的】基板内部にコンデンサが内蔵された配線基板において、信号ビア間の容量およびインダクタンスを低減することができる配線基板を提供すること。
【構成】配線基板１は、その主面１Ａに密集領域ＭＲを形成する第１接続端子３Ｐおよび第２接続端子３Ｇを備える。また、内部に、電源電極層２９等、接地電極層３０等、および高誘電体層７６等からなる内蔵コンデンサ１３を備える。高誘電体層７６等を貫通する信号ビア１９Ｖの間には接地ビア１８を設け、信号ビア１９Ｖ間の容量およびインダクタンスをシールド効果により低減する。



1

【特許請求の範囲】

【請求項１】主面と裏面とを有する配線基板であって、上記主面に形成され、ＩＣチップの端子と接続するための多数の接続端子であって、多数の第１接続端子、第２接続端子、および第３接続端子を含み、

上記第１接続端子および第２接続端子の少なくとも一部は、上記第１接続端子と第２接続端子とが密集する密集領域をなして配置された接続端子と、

上記裏面に形成された第１外部接続端子、第２外部接続端子、および第３外部接続端子からなる外部接続端子と、

上記配線基板の内部に、高誘電体層を介して少なくとも上記密集領域を厚さ方向に投影した投影密集領域に積層され、コンデンサの電極を構成する複数の略平板状の導体層であって、

第１貫通孔を有し、電源電位に接続される第１導体層と、

第２貫通孔を有し、接地電位に接続される第２導体層と、

上記第１接続端子と上記第１導体層と上記第１外部接続端子とを接続し、上記第２貫通孔内に位置し、第２導体層と絶縁する第１接続配線と、

上記第２接続端子と上記第２導体層と上記第２外部接続端子とを接続し、上記第１貫通孔内に位置し、第１導体層と絶縁する第２接続配線と、

上記密集領域を厚さ方向に投影した投影密集領域の外側の周縁領域内の高誘電体層を貫通するビア導体を含み、

上記第３接続端子と上記第３外部接続端子とを接続する信号伝達用の第３接続配線と、からなり、

上記ビア導体相互間には、上記高誘電体層を貫通する接地電位に接続される接地ビア導体が形成されていることを特徴とする配線基板。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、基板内部に高誘電体層と電極層とからなるコンデンサが内蔵された配線基板に関し、特に高誘電体層を貫通する部位での信号配線間のキャパシタンスおよびクロストークノイズを低減させる構造に関する。

【０００２】

【従来の技術】従来より、複数の絶縁層と導体層を交互に積層して形成され、主面側にＩＣチップ等を、または裏面側にマザーボード等を接続することができ、基板内部にコンデンサが内蔵形成された配線基板が知られている。このような配線基板においては、主面側にＩＣチップ等の接続端子に対応したハンダバンプ（接続端子）が多数形成され、一方、裏面側には、マザーボード等の接続端子に対応した接続パッド（外部接続端子）が多数形成されている。

【０００３】このうち、主面に形成されたハンダバンプ

2

は電源電位と接続する電源バンプ（第１接続端子）と、接地電位を接続する接地バンプ（第２接続端子）と、信号を出入力するための信号バンプ（第３接続端子）とをそれぞれ多数有している。これらの接続端子は、主面に略格子状に密集して配置されている。特に、電源バンプと接地バンプとは略格子状に密集した密集領域をなしている。

【０００４】また、内蔵されたコンデンサは、上記密集領域を含んで形成された第１導体層および第２導体層と、第１導体層および第２導体層の間に挟まれた高誘電体層からなる。第１導体層は第１接続配線を介して電源バンプ（第１接続端子）および電源パッド（第１外部接続端子）と接続されている。第１接続配線は、第２導体層に形成された第２貫通孔内を通るため、第２導体層とは絶縁されている。また、第２導体層は第２接続配線を介して接地バンプ（第２接続端子）および接地パッド（第２外部接続端子）と接続されている。第２接続配線は第１導体層に形成された第１貫通孔内を通り、第１導体層とは絶縁されている。

【０００５】ところで、このようなコンデンサ内蔵型配線基板は、多数積層された絶縁層の一部を高誘電体材料からなる高誘電体層とし、この高誘電体層を電極層により挟持した構造の内蔵コンデンサを有している。各電極層とハンダバンプとを結ぶ接続配線のインダクタンスを下げるため、内蔵コンデンサはハンダバンプ（接地バンプ、電源バンプ）の真下部分、すなわち、密集領域を厚さ方向に投影した投影密集領域に設けられる。このような構造の配線基板において、投影密集領域の外側の周縁領域においては、電極層を設けず、信号用の配線（ビア導体）等が多数形成される。

【０００６】

【発明が解決しようとする課題】しかし、電極層が設けられない周縁領域においても、絶縁層はコンデンサ部分と同じ高誘電体層からなるため、高誘電体層表面に設けられる信号用の配線やビア導体相互間でキャパシタンスが大きくなり、また、隣接する信号用の配線やビア間でクロストークノイズが発生するという問題がある。

【０００７】本発明は上記問題点を解決するためになされたものであって、本発明の目的は、内蔵コンデンサの外側の周縁領域において、信号配線間のキャパシタンスおよびクロストークノイズを低減させることができるコンデンサ内蔵型配線基板を提供することにある。

【０００８】

【課題を解決するための手段】しかして、その手段は、主面と裏面とを有する配線基板であって、上記主面に形成され、ＩＣチップの端子と接続するための多数の接続端子であって、多数の第１接続端子、第２接続端子、および第３接続端子を含み、上記第１接続端子および第２接続端子の少なくとも一部は、上記第１接続端子と第２接続端子とが密集する密集領域をなして配置された接続

端子と、上記裏面に形成された第１外部接続端子、第２外部接続端子、および第３外部接続端子からなる外部接続端子と、上記配線基板の内部に、高誘電体層を介して少なくとも上記密集領域を厚さ方向に投影した投影密集領域に積層され、コンデンサの電極を構成する複数の略平板状の導体層であって、第１貫通孔を有し、電源電位に接続される第１導体層と、第２貫通孔を有し、接地電位に接続される第２導体層と、上記第１接続端子と上記第１導体層と上記第１外部接続端子とを接続し、上記第２貫通孔内に位置し、第２導体層と絶縁する第１接続配線と、上記第２接続端子と上記第２導体層と上記第２外部接続端子とを接続し、上記第１貫通孔内に位置し、第１導体層と絶縁する第２接続配線と、上記密集領域を厚さ方向に投影した投影密集領域の外側の周縁領域内の高誘電体層を貫通するビア導体を含み、上記第３接続端子と上記第３外部接続端子とを接続する信号伝達用の第３接続配線と、からなり、上記ビア導体相互間には、上記高誘電体層を貫通する接地電位に接続される接地ビア導体が形成されていることを特徴とする配線基板である。

【０００９】上記配線基板によれば、高誘電体層を貫通する信号用のビア導体相互の間に接地電極に繋がった接地ビア導体を形成したため、シールド効果により、信号用のビア導体間のキャパシタンスおよびクロストークノイズを低減できる。

【００１０】なお、高誘電体層としては、電極となる導体層や高誘電体層ではない絶縁層などの材質、製法等を勘案して選択すればよいが、$BaTiO_3$の他、たとえば、$PbTiO_3$、$PbZrO_3$、TiO_2、$SrTiO_3$、$CaTiO_3$、$MgTiO_3$、$KNbO_3$、NbO_3、$NaTiO_3$、$KTaO_3$、$RbTaO_3$、$(Na_{1/2}Bi_{1/2})TiO_3$、$Pb(Mg_{1/2}W_{1/2})O_3$、$(K_{1/2}Bi_{1/2})TiO_3$などを主成分とした高誘電率セラミックが挙げられる。また、アルミナ、窒化アルミニウム、ムライト、ガラスセラミックなどのセラミックに、あるいはエポキシ樹脂やポリイミド樹脂、ＢＴ樹脂などの樹脂に、上記高誘電率セラミックのフィラーを添加した複合材料なども用いることができる。これらは要求されるコンデンサの静電容量その他に応じて適宜選択すればよい。

【００１１】

【発明の実施の形態】以下、本発明の実施の形態を図面を参照しつつ説明する。本実施形態の配線基板１について、図１（ａ）に平面図を、図１（ｂ）に側面図を、図２に部分拡大断面図を示す。この配線基板１は、図１（ｂ）に示すように主面１Ａと裏面１Ｂを有し、略矩形状の略板形状をなしている。配線基板１の主面１Ａ側には図中に破線で示すＩＣチップ'ＣＨ搭載することができる一方、裏面１Ｂ側には、図中に破線で示すマザーボードＭＢなど他の配線基板を接続することができる。

【００１２】搭載予定のＩＣチップ'ＣＨは、配線基板１とのＩＣ接続端子として、ハンダバンプ'Ｔを多数備えている。このハンダバンプ'Ｔは、信号を入出力するための信号バンプ'ＴＳの他、電源電位を受け入れる電源バンプ'ＴＰ、および接地電位を受け入れる接地バンプ'ＴＧを多数有している。一方、この配線基板１を接続する予定のマザーボードＭＢも、配線基板１との接続端子として、信号バンプ'ＵＳ、電源バンプ'ＵＰ、および接地バンプ'ＵＧ等のハンダバンプ'Ｕを多数有している。

【００１３】本実施形態の配線基板１は、図１（ｂ）に示すように、その主面１Ａに、ＩＣチップ'ＣＨのハンダバンプ'Ｔと接続する接続端子として、多数のハンダバンプ３を有し、また、裏面１Ｂに、マザーボードＭＢのハンダバンプ'Ｕと接続する接続端子として、多数の接続パッド（外部接続端子）５を有している。このうち、主面１Ａに形成された接続端子は、ＩＣのハンダバンプ'Ｔ（電源バンプ'ＴＰ、接地バンプ'ＴＧ、信号バンプ'ＴＳ）に対応した電源バンプ（第１接続端子）３Ｐ、接地バンプ（第２接続端子）３Ｇ、および信号バンプ（第３接続端子）３Ｓをそれぞれ有している。これらのハンダバンプ'３は、図１（ａ）に示すように、配線基板１の主面１Ａに略格子状に並び、略矩形状のバンプ領域ＢＲを形成している。さらに詳細にいうと、このバンプ領域ＢＲの略中央には、多数の電源バンプ'３Ｐと接地バンプ'３Ｇとが、１５０μｍの格子間隔で互い違いに略格子状に密集して並んだ略矩形状の密集領域ＭＲが形成されている。また、バンプ領域ＢＲのうち密集領域ＭＲを取り囲む領域に、信号バンプ'３Ｓ、電源バンプ'３Ｐ、および接地バンプ'３Ｇが格子状に多数並んだ周囲領域ＳＲが形成されている。

【００１４】一方、裏面１Ｂに形成された接続パッド５も、マザーボードのハンダバンプ'Ｕに対応した信号パッド５Ｓ、電源パッド５Ｐ、および接地パッド５Ｇをそれぞれ多数有し、略矩形状のパッド領域を形成している。そして、パッド領域の略中央には、多数の電源パッド５Ｐと接地パッド５Ｇが互い違いに略格子状に配置されている。また、それらの周囲には、信号パッド５Ｓ、電源パッド５Ｐ、および接地パッド５Ｇが多数配置されている。

【００１５】この配線基板１は、図２に示すように、主面１Ａを形成する第１絶縁層７１から裏面１Ｂを形成する第１１絶縁層８１まで全部で１１層の絶縁層が積層されたものである。そして、これらの絶縁層７１～８１の層内や層間にはそれぞれビア導体や配線パターンが形成されている。

【００１６】この配線基板１の内部構造を大きく分類すると、第１絶縁層７１～第５絶縁層７５からなる展開部９と、$BaTiO_3$を主成分とする高誘電体層からなる第６絶縁層７６～第１０絶縁層８０等からなる内蔵コンデンサ１３とに分けられる。なお、絶縁層７１～７５、および８１の材質は特に限定されないがセラミックやガ

ラスセラミックなどを好適に用いることができる。

【００１７】このうち展開部９は、主として、前述したバンプ領域ＢＲのうち、周縁領域ＳＲに形成されたハンダバンプ３とこれらと対応する接続パッド５とを電気的に接続させるために、これらのハンダバンプと接続する配線、特に信号バンプ３Ｓと信号パッド５Ｓとを電気的に接続するためにの信号配線（第３接続配線）１９等を引き回して配線基板１の周縁方向へ展開（ファンアウト）させるためのものである。一方、図２に示す投影密集領域ＴＭＲ内では、電源バンプ３Ｐに接続した電源配線（第１接続配線）１５、および、接地バンプ３Ｇに接続した接地配線（第２接続配線）１７がそれぞれ主面１Ａ側から裏面１Ｂ側へ向かって厚さ方向に延びている。

【００１８】また、内蔵コンデンサ１３は、主として、投影密集領域ＴＭＲ内において、電源バンプ３Ｐから延びた電源配線（第１接続配線）１５が電源電極層（第１導体層）２９、３１、３３に接続しており、また、接地バンプ３Ｇから延びた接地配線（第２接続配線）１７が接地電極層（第２導体層）３０、３２、３４に接続している。このように各電極層に接続するための電源配線１５、接地配線１７を投影密集領域ＴＭＲに集中させたために電源配線１５、接地配線１７のインダクタンスを低減できる。

【００１９】また、投影密集領域ＴＭＲ内においては、上述した通り、電源配線１５および接地配線１７が集中するために、接地配線１７と電源電極層２９、３１、３３とを絶縁するために電源電極層２９、３１、３３に設けられた第１貫通孔２９Ｋ、３１Ｋ、３３Ｋも密集して形成されることとなる。同様に、電源配線１９と接地電極層３０、３２、３４とを絶縁するために接地電極層３０、３２、３４に設けられた第２貫通孔３０Ｋ、３２Ｋ、３４Ｋも密集して形成されることとなる。

【００２０】具体的には、投影密集領域ＴＭＲ内においては、電源配線１５と、これと隣接する接地配線１７との間隔は、例えば１５０μｍ～４５０μｍ程度に設定されている。したがって、第１貫通孔２９Ｋ、３１Ｋ、３３Ｋ、第２貫通孔３０Ｋ、３２Ｋ、３４Ｋとの間隔も、１５０μｍ～４５０μｍ程度に設定されている。

【００２１】次に、投影密集領域ＴＭＲの周囲に設けられた配線基板内部の周縁領域ＴＳＲについて説明する。周縁領域ＴＳＲにおいては、展開部９にハンダバンプ３から展開された配線が形成されており、特に、信号バンプ３Ｓから延びて形成された信号配線１９が集中的に配置されている。内蔵コンデンサ１３周縁部分においては、信号配線１９は、高誘電体層７６～８０を貫通する信号ビア１９Ｖを介して、いずれの電極層とも絶縁されつつ、信号パッド５Ｓとそれぞれ接続されている。

【００２２】信号配線１９は、相互の間隔が１ｍｍ～１．５ｍｍ程度（例えば１．２７ｍｍ）に設定されている。このように信号配線１９は、電源配線１５や接地配線１７と比べると、比較的間隔が広くなるように展開部９で展開（ファンアウト）されている。しかし、信号配線１９は、高誘電体層７６～８０を貫通するので、特に隣接する信号ビア１９Ｖ同士のキャパシタンスが大きくなり、クロストークノイズが大きくなりがちである。

【００２３】これに対し、本実施形態の配線基板１においては、図３の平面図に示すように、信号ビアＶ（φ７５μｍ）の間隔１．２７ｍｍの場合で、信号ビア１９Ｖの中間に接地ビア１８を設けている。なお、高誘電体層７６～８０の誘電率は約５０００である。このような構造にすることにより、接地ビア１８によるシールド効果により、接地ビアを設けない場合の信号ビア間のキャパシタンスである２５．８ｐＦと比べ、信号ビア１９Ｖ間のキャパシタンスを０．１６ｐＦまで低減できる。また、クロストークノイズも、接地ビアを設けない場合の数％～１０％から、シールド効果により、０．１７％まで低減できる。

【００２４】さらに、本実施形態では、接地ビア１８の径（φ３００μｍ）を信号ビア１９Ｖの径（φ７５μｍ）よりも大きくしているので、信号ビア１９Ｖの径と同径にした場合よりも、信号ビア１９Ｖ間のキャパシタンスおよびクロストークノイズをより効果的に低減することができる。

【００２５】なお、信号ビア１９Ｖと接地ビア１８の配置の仕方は、図３の形態に限定されることなく、例えば、図４や図５に示すような配置も採用できる。すなわち、図４に示した構造では、図３のものと比べて信号ビア１９Ｖがより高密度に形成されている。また、図５に示した構造では、図３や図４に示したものに比べて、接地ビア１８が信号ビア１９Ｖを包囲するように列設されており、シールド効果がさらに強化されている。

【００２６】以上説明した通り、コンデンサを内蔵した配線基板において、コンデンサの周囲の高誘電体層を貫通する信号ビア相互間に、接地ビアを設けてあるため、信号ビア相互間の容量およびクロストークノイズを低減できる。さらに、接地ビアの径を信号ビアの径よりも大きくすると、隣接する信号ビア間の容量およびクロストークノイズの低減をより効果的に行うことができる。

【図面の簡単な説明】

【図１】本発明の実施形態に係る配線基板を示す図であり、（ａ）は平面図であり、（ｂ）は側面図である。

【図２】本発明の実施形態に係る配線基板の部分拡大断面図である。

【図３】本発明の実施形態に係る信号ビアおよび接地ビアの配置を示す平面図である。

【図４】図３とは異なる信号ビアおよび接地ビアの配置を示す平面図である。

【図５】図３、図４とは異なる信号ビアおよび接地ビアの配置を示す平面図である。

【符号の説明】

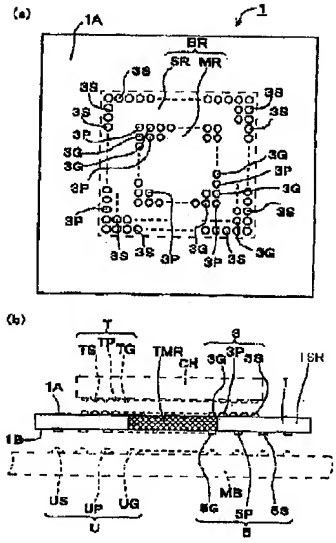
7

1　配線基板
3　ハンダバンプ（接続端子）
3Ｐ　電源バンプ（第１接続端子）
3Ｇ　接地バンプ（第２接続端子）
3Ｓ　信号バンプ（第３接続端子）
5　接続パッド（外部接続端子）
5Ｐ　電源パッド（第１外部接続端子）
5Ｇ　接地パッド（第２外部接続端子）
5Ｓ　信号パッド（第３外部接続端子）
9　展開部
１３　内蔵コンデンサ

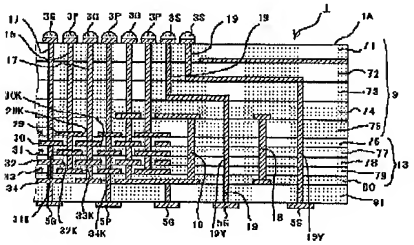
8

１５　電源配線（第１接続配線）
１７　接地配線（第２接続配線）
１８　接地ビア
１９　信号配線（第３接続配線）
１９Ｖ　信号ビア
２９、３１、３３　電源電極層（第１導電層）
３０、３２、３４　接地電極層（第２電極層）
２９Ｋ、３１Ｋ、３３Ｋ　第１貫通孔
３０Ｋ、３２Ｋ、３４Ｋ　第２貫通孔
10　７６～８０　高誘電体層

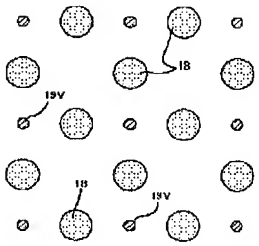
【図１】



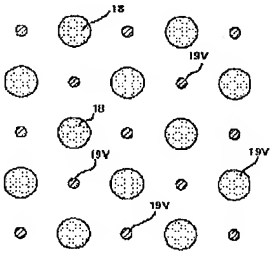
【図２】



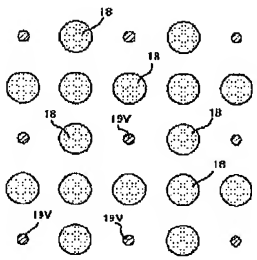
【図３】



【図４】



【図５】



フロントページの続き

(72)発明者　杉本　康宏
愛知県名古屋市瑞穂区高辻町14番18号　日本特殊陶業株式会社内

Ｆターム(参考)　5E346 AA13 AA15 AA42 AA43 BB02 BB03 BB04 BB06 BB16 BB20 CC17 CC31 CC40 FF01 FF45 HH01 HH04

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the structure of reducing the capacitance and cross talk noise between the signal wiring in the part which penetrates especially a high dielectric layer, about the wiring substrate by which the capacitor which consists of a high dielectric layer and an electrode layer was built in the interior of a substrate.
[0002]
[Description of the Prior Art] From before, the laminating of two or more insulating layers and conductor layers is carried out by turns, it is formed, a mother board etc. can be connected to a principal plane side at IC chip etc. and a rear-face side, and the wiring substrate by which built-in formation of the capacitor was carried out inside the substrate is known. In such a wiring substrate, many pewter bumps (end-connection child) corresponding to end-connection children, such as IC chip, are formed in a principal plane side, and, on the other hand, many connection pads (external end-connection child) corresponding to end-connection children, such as a mother board, are formed in the rear-face side.
[0003] Among these, the pewter bump formed in the principal plane has many power supply bumps (the 1st end-connection child) linked to power supply potential, grounding bumps (the 2nd end-connection child) who connect grounding potential, and signal bumps (the 3rd end-connection child) for carrying out the in-and-out force of the signal, respectively. These end-connection children crowd in a principal plane in the shape of an abbreviation grid, and are stationed. Especially a power supply bump and a grounding bump are making the high density field which crowded in the shape of an abbreviation grid.
[0004] Moreover, the built-in capacitor consists of a high dielectric layer inserted between the 1st conductor layer and the 2nd conductor layer which were formed including the above-mentioned high density field, and the 1st conductor layer and the 2nd conductor layer. The 1st conductor layer is connected with the power supply bump (the 1st end-connection child) and the power supply pad (the 1st external end-connection child) through the 1st connection wiring. Since the 1st connection wiring passes along the inside of the 2nd breakthrough formed in the 2nd conductor layer, it is insulated with the 2nd conductor layer. Moreover, the 2nd conductor layer is connected with the grounding bump (the 2nd end-connection child) and the grounding pad (the 2nd external end-connection child) through the 2nd connection wiring. The 2nd connection wiring passes along the inside of the 1st breakthrough formed in the 1st conductor layer, and is insulated with the 1st conductor layer.
[0005] By the way, many such capacitor built-in wiring substrates make a part of insulating layer by which the laminating was carried out the high dielectric layer which consists of high dielectric materials, and have the built-in capacitor of the structure which pinched this high dielectric layer by the electrode layer. In order to lower the inductance of the connection wiring which connects each electrode layer and a pewter bump, a built-in capacitor is formed in a just under [a pewter bump (a grounding bump, power supply bump)] portion, i.e., the projection high density field which projected the high density field in the thickness direction. In the wiring substrate of such structure, in the periphery field of the outside of a projection high density field, an electrode layer is not prepared but much wiring for signals (beer conductor) etc. is formed.
[0006]
[Problem(s) to be Solved by the Invention] however, the wiring for signals formed in a high dielectric-layer front face also in the periphery field in which an electrode layer is not prepared since an insulating layer consists of the same high dielectric layer as a capacitor portion and beer -- a conductor -- there is a problem that a cross talk noise occurs between the wiring for signals which capacitance becomes large and adjoins mutually, or beer
[0007] Made in order that this invention may solve the above-mentioned trouble, the purpose of this invention is in the periphery field of the outside of a built-in capacitor to offer the capacitor built-in wiring substrate which can reduce the capacitance and cross talk noise between signal wiring.
[0008]
[Means for Solving the Problem] Carry out a deer, and the means is a wiring substrate which has a principal plane and a rear face, and is formed in the above-mentioned principal plane. They are many end-connection children for connecting with the terminal of IC chip. Many 1st end-connection children, the [the 2nd end-connection child and] -- 3 end-connection child -- containing -- the [the above-mentioned 1st end-connection child and] -- some 2 end-connection children [at least] With the end-connection child who made the high density field where the above-mentioned 1st end-connection child and the 2nd end-connection child crowd, and has been stationed With the 1st external end-connection child formed in the above-mentioned rear face, the 2nd external end-connection child, and the external end-connection child who reaches and consists of a 3rd external end-connection child A laminating is carried out to the projection high density field which projected

the above-mentioned high density field on the interior of the above-mentioned wiring substrate in the thickness direction at least through the high dielectric layer. The 1st conductor layer which is two or more abbreviation plate-like conductor layers which constitute the electrode of a capacitor, has the 1st breakthrough, and is connected to power supply potential, The 1st connection wiring which has the 2nd breakthrough, connects the 2nd conductor layer connected to grounding potential, the above-mentioned 1st end-connection child and the 1st conductor layer of the above, and the above-mentioned 1st external end-connection child, is located in the 2nd breakthrough of the above, and is insulated with the 2nd conductor layer, The 2nd connection wiring which connects the above-mentioned 2nd end-connection child, the 2nd conductor layer of the above, and the above-mentioned 2nd external end-connection child, is located in the 1st breakthrough of the above, and is insulated with the 1st conductor layer, the beer which penetrates the high dielectric layer in the periphery field of the outside of the projection high density field which projected the above-mentioned high density field in the thickness direction -- including a conductor with the 3rd connection wiring for signal transduction which connects the above-mentioned 3rd end-connection child and the above-mentioned 3rd external end-connection child a shell -- the above-mentioned beer -- a conductor -- the grounding beer connected to the grounding potential which penetrates the above-mentioned quantity dielectric layer mutually -- it is the wiring substrate characterized by forming the conductor

[0009] the beer for signals which penetrates a high dielectric layer according to the above-mentioned wiring substrate -- the grounding beer connected with the grounding electrode among both conductors -- since the conductor was formed -- a shielding effect -- the beer for signals -- a conductor -- the capacitance and cross talk noise of a between can be reduced

[0010] Although what is necessary is to take into consideration the quality of the materials, such as an insulating layer which is not the conductor layer or high dielectric layer used as an electrode as a high dielectric layer, a process, etc., and just to choose, everything but BaTiO3 in addition, for example PbTiO3, PbZrO3, TiO2, SrTiO3, CaTiO3, MgTiO3, KNbO3, NbO3, NaTiO3, KTaO3, RbTaO3, TiO (Na1/2Bi1/2)3, Pb(Mg1/2W1/2) O3, (K1/2Bi1/2) The high dielectric constant ceramic which made TiO3 etc. the principal component is mentioned. Moreover, the composite material which added the filler of the above-mentioned quantity dielectric constant ceramic can be used for ceramics, such as an alumina, alumimium nitride, a mullite, and a glass ceramic, or resins, such as an epoxy resin, and polyimide resin, BT resin. What is necessary is just to choose these suitably according to the electrostatic capacity and others of the capacitor demanded.

[0011]

[Embodiments of the Invention] Hereafter, the gestalt of operation of this invention is explained, referring to a drawing. the wiring substrate 1 of this operation gestalt -- a side elevation is shown in drawing 1 (b), and a partial expanded sectional view is shown for a plan in drawing 1 (a) at drawing 2 This wiring substrate 1 has principal plane 1A and rear-face 1B, as shown in drawing 1 (b), and it is making the abbreviation rectangle-like **** configuration. While IC chip CH loading can be carried out, other wiring substrates, such as the mother board MB which is shown with a dashed line all over drawing and which is shown with a dashed line all over drawing, are connectable with the principal plane 1A side of the wiring substrate 1 at the rear-face 1B side.

[0012] The IC chip CH of a loading schedule is equipped with many pewter bumps T as an IC end-connection child with the wiring substrate 1. This pewter bump T has many grounding bumps TG who accept the power supply bump TP who accepts power supply potential besides the signal bump TS for outputting and inputting a signal, and grounding potential. On the other hand, the mother board MB which is due to connect this wiring substrate 1 also has many pewter bumps U, such as the signal bump US, the power supply bump UP, and the grounding bump UG, as an end-connection child with the wiring substrate 1.

[0013] The wiring substrate 1 of this operation gestalt has many connection pads (external end-connection child) 5 as an end-connection child who has many pewter bumps 3 in the principal plane 1A, and connects with it with the pewter bump U of a mother board MB at rear-face 1B as an end-connection child who connects with the pewter bump T of the IC chip CH, as shown in drawing 1 (b). Among these, the end-connection child formed in principal plane 1A has power supply bump (1st end-connection child) 3P corresponding to the pewter bump T of IC (the power supply bump TP, the grounding bump TG, signal bump TS), grounding bump (2nd end-connection child) 3G, and signal bump (3rd end-connection child) 3S, respectively. As shown in drawing 1 (a), these pewter bumps 3 rank with principal plane 1A of the wiring substrate 1 in the shape of an abbreviation grid, and form the abbreviation rectangle-like bump field BR. If it furthermore says a detail, the abbreviation rectangle-like high density field MR where much power supply bump 3P and grounding bump 3G were alternately close with the 150-micrometer lattice spacing in the shape of an abbreviation grid, and were located in a line is formed in the center of abbreviation of this bump field BR. Moreover, the circumference field SR where much signal bump 3S, power supply bump 3P, and grounding bump 3G were located in a line in the shape of a grid is formed in the field which encloses the high density field MR among the bump fields BR.

[0014] On the other hand, the connection pad 5 formed in rear-face 1B also has much signal pad 5S corresponding to the pewter bump U of a mother board, power supply pad 5P, and grounding pad 5G, respectively, and forms the abbreviation rectangle-like pad field. And in the center of abbreviation of a pad field, much power supply pad 5P and grounding pad 5G are alternately arranged in the shape of an abbreviation grid. Moreover, much signal pad 5S, power supply pad 5P, and grounding pad 5G are arranged at those circumferences.

[0015] As shown in drawing 2 , as for this wiring substrate 1, the laminating of the insulating layer of 11 layers is carried out in all to the 11th insulating layer 81 which forms rear-face 1B from the 1st insulating layer 71 which forms principal plane 1A. and -- between the inside of the layer of these insulating layers 71-81, or a layer -- respectively -- beer -- the conductor and the circuit pattern are formed

[0016] It will be divided into the expansion section 9 which consists of the 1st insulating layer 71 - the 5th insulating layer 75, and the built-in capacitor 13 which consists of the 6th insulating layer 76 which consists of a high dielectric layer which makes BaTiO3 a principal component - 10th insulating-layer 80 grade if the internal structure of this wiring substrate 1 is roughly classified. in addition, insulating-layer 71- although especially the quality of the material of 75 and 81 is not limited, it can use a ceramic, a glass ceramic, etc. suitably

[0017] Among these, in order for the expansion section 9 to connect electrically the pewter bump 3 formed in the periphery field SR mainly among the bump fields BR mentioned above, these, and the corresponding connection pad 5 It is for taking about the wiring which connects with these pewter bumps, especially the signal wiring (the 3rd connection wiring) 19 grade which connects electrically signal bump 3S and signal pad 5S and which is accumulated and boiled, and making it develop in the direction of a periphery of the wiring substrate 1 (fan-out). On the other hand, in the projection high density field TMR shown in drawing 2 , the power supply wiring (the 1st connection wiring) 15 linked to power supply bump 3P and the grounding wiring (the 2nd connection wiring) 17 linked to grounding bump 3G are prolonged in the thickness direction toward the rear-face 1B side from the principal plane 1A side, respectively.

[0018] Moreover, the grounding wiring (the 2nd connection wiring) 17 which the power supply wiring (the 1st connection wiring) 15 prolonged from power supply bump 3P in the projection high density field TMR had mainly connected the built-in capacitor 13 to the power supply electrode layers (the 1st conductor layer) 29, 31, and 33, and was prolonged from grounding bump 3G has connected with the grounding-electrode layers (the 2nd conductor layer) 30, 32, and 34. Thus, since the power supply wiring 15 for connecting with each electrode layer and the grounding wiring 17 were centralized on the projection high density field TMR, the inductance of the power supply wiring 15 and the grounding wiring 17 can be reduced.

[0019] Moreover, in order that the power supply wiring 15 and the grounding wiring 17 may concentrate as mentioned above in the projection high density field TMR, in order to insulate the grounding wiring 17 and the power supply electrode layers 29, 31, and 33, the 1st breakthrough 29K, 31K, and 33K prepared in the power supply electrode layers 29, 31, and 33 will also crowd, and will be formed. Similarly, in order to insulate the power supply wiring 19 and the grounding-electrode layers 30, 32, and 34, the 2nd breakthrough 30K, 32K, and 34K prepared in the grounding-electrode layers 30, 32, and 34 will also crowd, and will be formed.

[0020] Specifically, the interval of the power supply wiring 15 and the grounding wiring 17 which adjoins this is set as 150 micrometers - about 450 micrometers in the projection high density field TMR. Therefore, the interval with the 1st breakthrough 29K, 31K, and 33K and the 2nd breakthrough 30K, 32K, and 34K is also set as 150 micrometers - about 450 micrometers.

[0021] Next, the periphery field TSR inside the wiring substrate prepared in the circumference of the projection high density field TMR is explained. In the periphery field TSR, the wiring developed from the pewter bump 3 is formed in the expansion section 9, and the signal wiring 19 especially formed by being prolonged from signal bump 3S is arranged intensively. In a part for the 13 round marginal part of built-in capacitors, signal wiring 19 is connected with signal pad 5S, respectively, which electrode layer being insulated through signal beer 19V which penetrate the high dielectric layers 76-80.

[0022] The interval mutual in signal wiring 19 is set as 1mm - about (for example, 1.27mm) 1.5mm. Thus, signal wiring 19 is developed in the expansion section 9 so that an interval may become large comparatively compared with the power supply wiring 15 or the grounding wiring 17 (fan-out). However, since signal wiring 19 penetrates the high dielectric layers 76-80, the capacitance of signal beer 19V comrades which adjoin especially tends to become large, and the cross talk noise tends to become large.

[0023] On the other hand, in the wiring substrate 1 of this operation gestalt, as shown in the plan of drawing 3 , grounding beer 18 is provided in the middle of signal beer 19V by the case with an interval [of signal beer V (phi75micrometer)] of 1.27mm. In addition, the dielectric constant of the high dielectric layers 76-80 is about 5000. With such structure, compared with 25.8pF which is the capacitance between the signal beer when not preparing grounding beer, the capacitance between signal beer 19V can be reduced to 0.16pF by the shielding effect by grounding beer 18. Moreover, a cross talk noise can also be reduced from several % - 10% when not preparing grounding beer to 0.17% by the shielding effect.

[0024] Furthermore, with this operation gestalt, since the path (phi300micrometer) of grounding beer 18 is made larger than the path (phi75micrometer) of signal beer 19V, the capacitance and cross talk noise between signal beer 19V can be more effectively reduced rather than the case where it is made the path and the diameter of said of signal beer 19V.

[0025] In addition, arrangement as shown in drawing 4 or drawing 5 can also be used for the method of arrangement of signal beer 19V and grounding beer 18, for example, without being limited to the gestalt of drawing 3 . That is, with the structure shown in drawing 4 , signal beer 19V are formed more in high density compared with the thing of drawing 3 . Moreover, compared with what was shown in drawing 3 or drawing 4 , it is installed successively so that grounding beer 18 may surround signal beer 19V, and the shielding effect is further strengthened with the structure shown in drawing 5 .

[0026] Since grounding beer is prepared between [which penetrates the high dielectric layer around a capacitor] signal beer in the wiring substrate which built in the capacitor as explained above, the capacity and the cross talk noise between signal beer can be reduced. Furthermore, if the path of grounding beer is made larger than the path of signal beer, reduction of the capacity between adjoining signal beer and a cross talk noise can be performed more effectively.

[Translation done.]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] It is the wiring substrate which has a principal plane and a rear face, and they are many end-connection children for being formed in the above-mentioned principal plane and connecting with the terminal of IC chip. the [many 1st end-connection children, the 2nd end-connection child, and] -- 3 end-connection child -- containing -- the [the above-mentioned 1st end-connection child and] -- the end-connection child who some 2 end-connection children [at least] made the high density field where the above-mentioned 1st end-connection child and the 2nd end-connection child crowd, and has been stationed the [the 1st external end-connection child formed in the above-mentioned rear face, the 2nd external end-connection child, and] -- 3 external end-connection child The 1st conductor layer which is the wiring substrate equipped with the above, has the 1st breakthrough, and is connected to power supply potential, The 1st connection wiring which has the 2nd breakthrough, connects the 2nd conductor layer connected to grounding potential, the above-mentioned 1st end-connection child and the 1st conductor layer of the above, and the above-mentioned 1st external end-connection child, is located in the 2nd breakthrough of the above, and is insulated with the 2nd conductor layer, The 2nd connection wiring which connects the above-mentioned 2nd end-connection child, the 2nd conductor layer of the above, and the above-mentioned 2nd external end-connection child, is located in the 1st breakthrough of the above, and is insulated with the 1st conductor layer, the beer which penetrates the high dielectric layer in the periphery field of the outside of the projection high density field which projected the above-mentioned high density field in the thickness direction -- including a conductor with the 3rd connection wiring for signal transduction which connects the above-mentioned 3rd end-connection child and the above-mentioned 3rd external end-connection child a shell -- the above-mentioned beer -- a conductor -- the grounding beer connected to the grounding potential which penetrates the above-mentioned quantity dielectric layer mutually -- it is characterized by forming the conductor

---

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

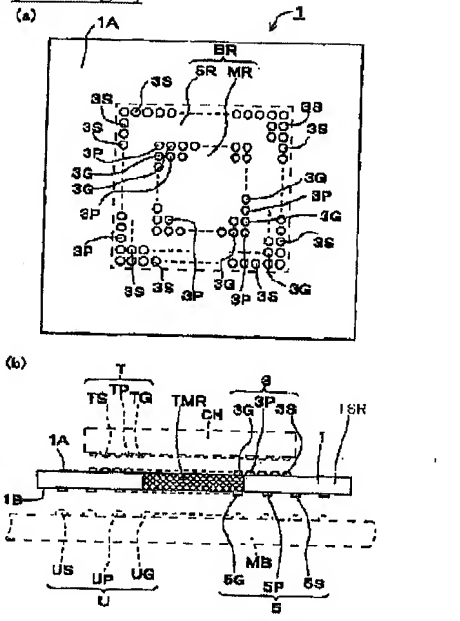
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the wiring substrate concerning the operation gestalt of this invention, and (a) is a plan and (b) is a side elevation.
[Drawing 2] It is the partial expanded sectional view of the wiring substrate concerning the operation gestalt of this invention.
[Drawing 3] It is the plan showing arrangement of the signal beer concerning the operation gestalt of this invention, and grounding beer.
[Drawing 4] Drawing 3 is the plan showing arrangement of different signal beer and grounding beer.
[Drawing 5] Drawing 3 and drawing 4 are the plans showing arrangement of different signal beer and grounding beer.
[Description of Notations]
1 Wiring Substrate
3 Pewter Bump (End-Connection Child)
3P Power supply bump (the 1st end-connection child)
3G Grounding bump (the 2nd end-connection child)
3S Signal bump (the 3rd end-connection child)
5 Connection Pad (External End-Connection Child)
5P Power supply pad (the 1st external end-connection child)
5G Grounding pad (the 2nd external end-connection child)
5S Signal pad (the 3rd external end-connection child)
9 Expansion Section
13 Built-in Capacitor
15 Power Supply Wiring (1st Connection Wiring)
17 Grounding Wiring (2nd Connection Wiring)
18 Grounding Beer
19 Signal Wiring (3rd Connection Wiring)
19V Signal beer
29, 31, 33 Power supply electrode layer (the 1st conductive layer)
30, 32, 34 Grounding-electrode layer (the 2nd electrode layer)
29K, 31K, 33K The 1st breakthrough
30K, 32K, 34K The 2nd breakthrough
76-80 Quantity dielectric layer

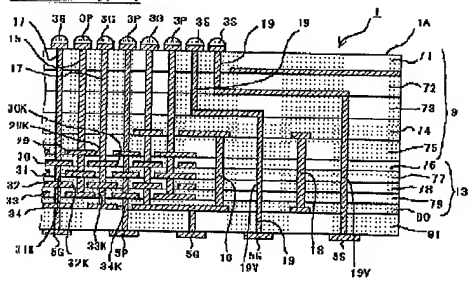
[Translation done.]

DRAWINGS

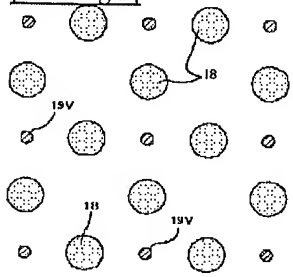
[Drawing 1]



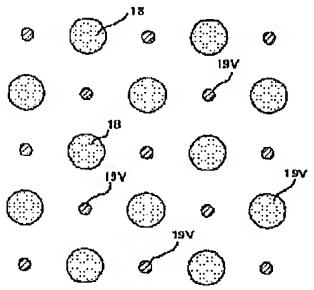
[Drawing 2]



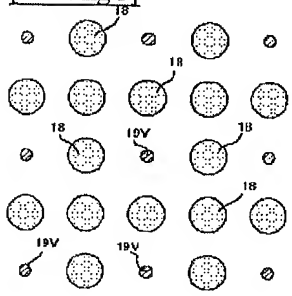
[Drawing 3]



[Drawing 4]



[Drawing 5]



[Translation done.]